Reset-While-Address (RWA) Driving Scheme for High-Speed Address in AC Plasma Display Panel With High Xe Content

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***Abstract*—A new reset while-address (RWA) driving scheme for a single scan of an XGA grade (1024 × 768) ac-plasma display panel (PDP) is proposed to improve the address discharge characteristics with a high Xe gas mixture (15%). To solve the conventional address problem of the gradual decrease in priming particles during an address period, the falling ramp waveform in the reset period is separated into two parts; the first part is applied at the beginning of the reset period and provides the priming particles during the first half of the address period, while the second part is applied in the middle of the address period to provide an additional supply of priming particles during the second half of the address period. As a result of adopting the proposed RWA driving scheme, address discharges were successfully produced within a 1.0-μs pulsewidth due to the presence of priming particles throughout the address period.**

***Index Terms*—AC-plasma display panel (PDP), high-speed address, high Xe content, plasma display panel (PDP), reset-while-address (RWA).**

I. Introduction

THE COST of current plasma display panel televisions (PDP-TVs) urgently needs to be lowered to a reasonable price to capture the digital TV consumer market [1]. The dual scan driving method for XGA-grade PDPs that uses two pairs of address driver ICs to address the two parts of the screen is one of the high price factors of PDP-TVs when compared with a single scan driving method [2]. However, with current technology, it is difficult to display a full high-definition panel using only a single scan method [3], due to the weak address discharge or address discharge failure, resulting from the lack of priming particles, especially during the second half of the address period. Moreover, the production of the address discharge is more difficult under high Xe gas mixture conditions without priming particles [4], [5]. Thus, improving the address discharge characteristics with a high Xe (>10%) gas mixture is very important and strongly depends on how the priming particles are used in the address discharge [6]. As for the firing voltage with an increase in the Xe contents, it is well known that the increase in the Xe concentration results in a reduced effective secondary electron emission coefficient and thus in an increase of the firing voltage [7]. It is thought that the presence of the priming particles can compensate the reduced effective secondary electron emission coefficient caused by the increase in the Xe concentration. It has been recently reported that high speed addressing ($< 1\ \mu$s) can be obtained in an ac-PDP with a Xe (4%) gas mixture using the priming particles from the adjacent cells [8]. However, the use of priming particles from adjacent cells causes a misfiring discharge and increases the background light. Furthermore, this type of driving method [8] is too complex for an address display-separate (ADS) driving scheme. The merit of the ADS driving scheme is the separation of address and sustain-periods, which facilitates the simple design of the driving pulse and also obtains the resultant low cost driving and stable discharge [9]–[11]. Moreover, the researches on the high speed driving under the high Xe (>10%) content have been hardly done, even though lots of researches on the improvement of the address discharge characteristics have been done under the low Xe (<10%) content so far [12]–[14].

Accordingly, this study presents a new reset while-address (RWA) driving scheme that provides an additional supply of priming particles during an address period without any side effects in a 42-in XGA grade PDP with a high Xe (15%) gas mixture under the ADS driving scheme. In the proposed RWA driving method, the conventional falling ramp waveform in the reset period is simply divided into two parts. As such, the total reset time for the proposed RWA driving method is the same as that for the conventional driving method. The first part of the falling ramp waveform is applied at the beginning of the reset period to provide priming particles during the first half of the address period, while the second part of the falling ramp waveform is applied midway through the address period to provide an additional supply of priming particles during the second half of the address period. When adopting the proposed RWA driving method, the address discharge time lags are examined and compared with those when using the conventional driving method.

II. Experimental Set-Up

Fig. 1 shows the discharge cell structure of the 42-in XGA-grade PDP used in this study with a gas mixture of Ne-Xe (15%)–He (35%) and pressure of 450 torr. The detailed specifications are listed in Table I. To compare the reset and address discharge characteristics for the conventional and proposed driving schemes, the IR (828 nm) emission waveform during an address period and the address discharge delay time, such as a formative and statistical delay time, were measured for both driving schemes using a photosensor

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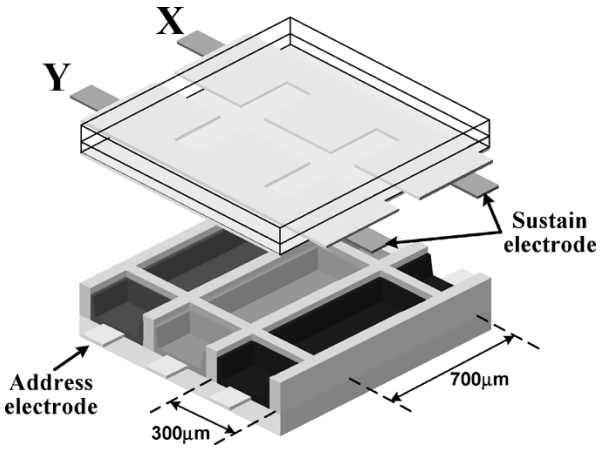

Fig. 1. Schematic diagram of single pixel in AC-PDP used in current study.

TABLE I
PANEL SPECIFICATIONS USED IN CURRENT STUDY

Front		Rear	
ITO width	200 μm	Address electrode width	150 μm
ITO gap	75 μm	Barrier rib height	120 μm
One cell pitch		900μm x 700μm	

amplifier (C6386). In addition, the background luminance and IR emission waveforms emitted during a reset period were also measured to compare the reset discharge characteristics for the conventional and proposed driving schemes. A color analyzer (CA-100 PLUS) was used to measure the luminance.

III. CONVENTIONAL DRIVING SCHEME

In the conventional driving scheme, the reset procedure is carried out simultaneously for the entire PDP within 200 μs, whereas the address procedure is carried out line by line from the scan line Y_1 to Y_{2n} for the entire PDP within 1000 μs after the reset procedure, as shown in Fig. 2(a). Fig. 2(b) then shows the conventional driving waveforms for the 42-in XGA grade PDP with a high Xe (15%) gas mixture corresponding to the reset, address, and sustain-periods, along with the IR waveforms measured during the application of the rising and falling ramp waveform in the reset period. In general, when applying the rising ramp pulse with a set-up voltage, V_{set} to the scan (Y) electrode in the reset period, negative wall charges are accumulated on the scan (Y) electrode, whereas positive wall charges are accumulated on the sustain (X) and address (A) electrodes. In the case of off-cells with no address discharge, the wall voltage difference between the sustain (X) and scan (Y) electrodes easily induces a misfiring discharge in the sustain-period. Accordingly, to avoid a misfiring discharge in the off-cells in the sustain-period, the proper amount of wall charges needs to be erased prior to the address discharge by applying the falling ramp and positive bias voltage, V_b to the scan (Y) and sustain (X) electrodes, respectively. The IR waveforms measured during the application of the falling ramp waveform are also shown in the lower part of Fig. 2(b), where the minimum voltage level of the falling ramp waveform is -100 V, as shown in Fig. 2(b). The wall charges erased

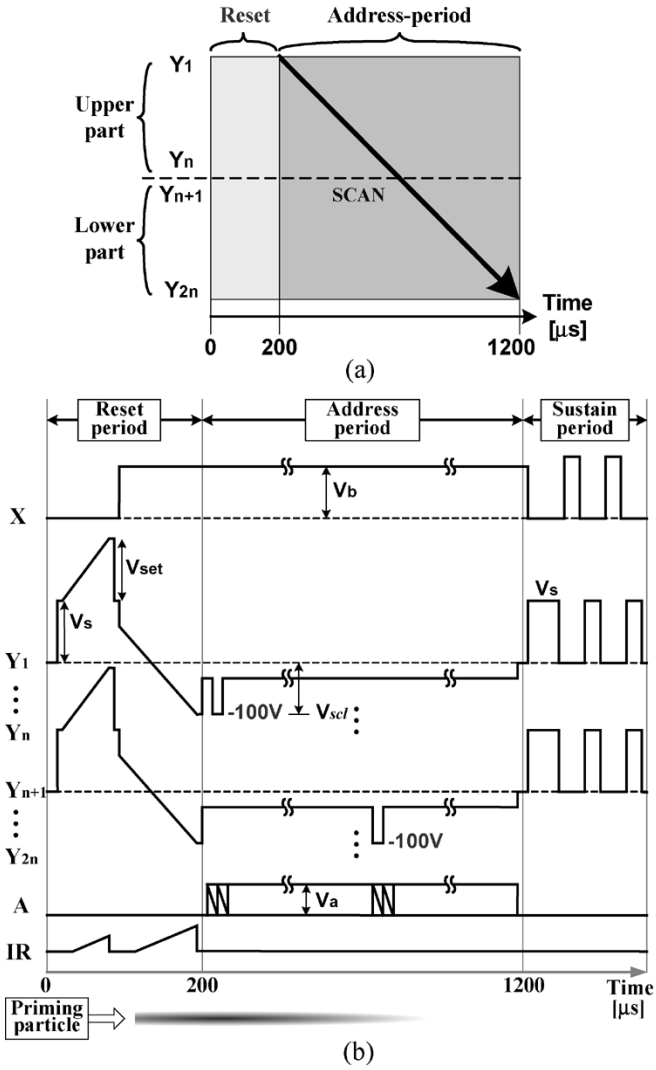

Fig. 2. (a) Schematic diagram of reset and address procedures and (b) corresponding conventional driving waveforms and related IR emission and schematic diagram of priming particle distribution during address period with conventional driving scheme.

during the ramp falling period act as priming particles that facilitate the address discharge in the address period, which means that the falling ramp pulse plus the positive bias voltage, V_b in the reset period play a role in producing the priming particles prior to the address discharge. It is expected that these priming particles contribute to improving the address discharge characteristics, especially with a high Xe gas mixture [4], [5]. The priming particles consist of the charged particles and the metastable species. It is well-known that the lifetimes of the charged particles are short, whereas those of the metastable species are relatively long. Nonetheless, it is very difficult to measure directly the density profile of the priming particles within micro-discharge cells, even though there has been a recent report that the decay characteristics of the charged and metastable species in PDP cells was measured in Ne+ Xe (4%) gas mixture at 500 torr [15]. However, even in [15], only the variation in the minimum sustain voltage was measured under the assumption that the disappearance of the priming particles with an elapse of time results in the variation in the minimum sustain voltage. Furthermore, the lifetimes of the priming

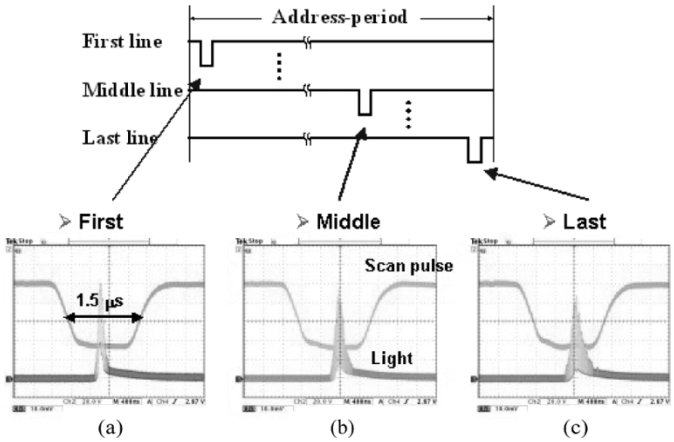

Fig. 3. Scan voltage and IR (828 nm) emission waveforms measured during address period at (a) first, (b) middle, and (c) last scan time when applying conventional driving waveform with address voltage of 70 V and scan pulsewidth of 1.5 μs.

particles strongly depends on the gas chemistry, pressure, cell geometry, cell size, MgO layer, and so on. Accordingly, in this paper, the address discharge time lags are measured with an elapse of time after the reset discharge so as to investigate the changes in the density profile of the priming particles under the assumption that the variations in the density profile of the priming particles result in the changes in the address discharge time lags during an address period [6].

Fig. 3(a)–(c) shows the light waveforms measured at the (a) first, (b) middle, and (c) last scan time during an address period when applying an address pulse with an amplitude of 70 V and width of 1.5 μs using the conventional driving scheme in Fig. 2(b). As shown in Fig. 3, it was observed that the address discharge intensity became weaker and also the address discharge time lag became longer with an elapse of time after the reset discharge. As mentioned before, these changes in the address discharge characteristics after the reset discharge are thought to be mainly due to the variations in the priming particles, such as the charged particles and metastable species, with an elapse of time after the reset discharge [6]. Fig. 4(b) illustrates the changes in the address discharge time lags measured at the time intervals of 100 μs ranging from 200 to 1100 μs during an address period after the reset discharge when applying the conventional driving waveforms shown in Fig. 2(b), where the measured discharge time lag, t_d is defined as the sum of the formative time lag t_f and statistical time lag t_s, i.e., $t_d = t_f + t_s$ as shown in Fig. 4(a) [5], [12]. As shown in Fig. 4(b), the address discharge time lags were increased slightly until 600 μs, but increased much after 600 μs, and almost saturated after 800 μs, which would deduce that the priming particles mostly disappeared after the middle scan time due to the lapse of time from the generation of the priming particles during the reset period. The reduction of priming particles during an address period causes an increase in the address voltage and address discharge failure. When applying an address pulse with an amplitude of 70 V and width of 1.0 μs using the conventional driving scheme in Fig. 2(b), no address discharge was produced during the second half of the address period with a high Xe (15%) content. Consequently, as displayed in the simple schematic density profile of

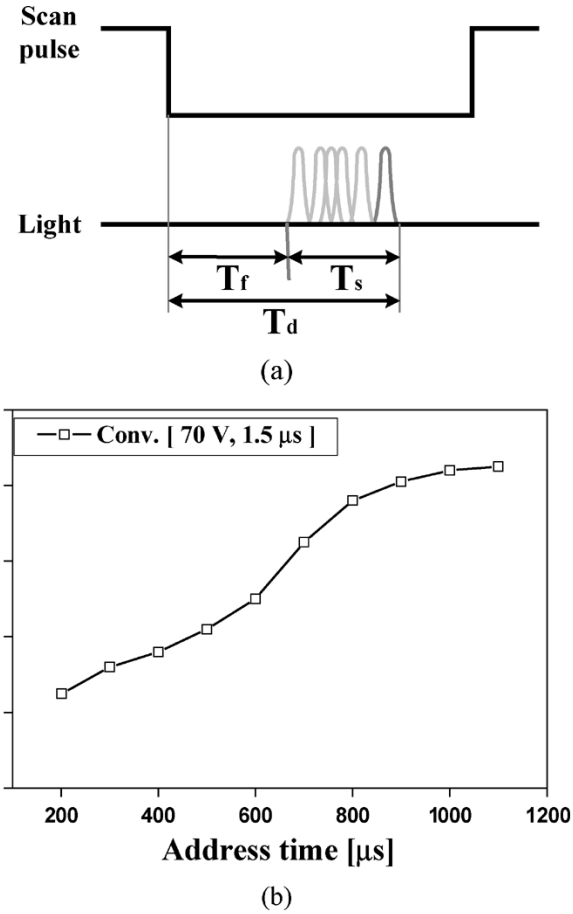

Fig. 4. (a) Address discharge time lag t_d expressed as a sum of formative time lag t_f and statistical time lag t_s, and (b) changes in address discharge time lags measured at time intervals of 100 μs ranging from 200 to 1100 μs during address period after reset discharge when applying conventional driving waveforms shown in Fig. 2(b).

the priming particles in the lower part of Fig. 2(b), the address discharge characteristics will deteriorate due to the reduction of the priming particles after the middle of the address period. Thus, if the priming particles can be provided once more in the middle of the address period, it is expected that the address discharge characteristics will be much improved, especially after the middle of the address period with a high Xe (>10%) gas mixture.

IV. Proposed RWA Driving Scheme for High-Speed Address With High Xenon Gas Concentration

Different address voltage margins can be induced depending on the difference in the scan time with the conventional driving scheme. As mentioned above, different address voltage margins are mainly due to the gradual decrease in the priming particles that have been generated in the reset period. In particular, the measurement of the address discharge time lags illustrates that the address discharge characteristics deteriorate from the middle to the last scan period. Thus, it was expected that an additional supply of priming particles in the middle of an address period would contribute to improving the address discharge characteristics with a high Xe content from the middle to the last scan time. As such, the proposed driving scheme, i.e., the RWA

driving scheme, was designed to provide an additional supply of priming particles in the middle of the address period, as shown in Fig. 5(a) and (b). The RWA driving scheme means that another reset procedure is carried out once more during an address period. That is to say, the RWA driving scheme does not mean that the reset and address procedures are not separated.

In the proposed RWA driving scheme, the conventional reset period is divided into two periods, the first reset and second reset periods, by separating the falling ramp pulse of the conventional reset waveform into two parts, which also means that the conventional address period is divided into two periods, the first address and second address periods. Unlike the conventional driving scheme in Fig. 2(a), the reset and address procedure in Fig. 5(a) shows that the first address procedure is carried out line by line from scan line Y_1 to Y_n only in the upper part of the PDP after the first reset procedure is simultaneously carried out for the entire PDP (equals the upper part plus the lower part), where the first address time is about 400 μs and the first reset time is about 180 μs. Meanwhile, the second address procedure is carried out line by line from the scan line Y_{n+1} to Y_{2n} only in the lower part of the PDP after the second reset procedure is simultaneously carried out for the entire PDP, where the second address time is about 400 μs and second reset time is about 20 μs.

Fig. 5(b) shows the proposed RWA driving scheme applied to the 42-in XGA grade PDP with a high Xe (15%) gas mixture, along with the IR waveforms measured during the first and second reset periods. The first falling ramp waveform with a minimum voltage level of -70 V in the first reset period supplies the priming particles during the first half of the address period from the first to the n^{th} scan line. Thereafter, the second falling ramp with a minimum voltage level of -100 V in the second reset period provides an additional supply of priming particles during the second half of the address period from the $(n+1)^{\text{th}}$ to the $2n^{\text{th}}$ scan line. The second ramp waveform in the second reset period applied between the first and second address periods is the tail part of the conventional falling ramp waveform, which means that the shape of the proposed falling ramp waveform (i.e., the first falling ramp waveform in the first reset period, plus the second falling ramp waveform in the second reset period) is exactly the same as that of the conventional falling ramp waveform. Thus, in the proposed RWA driving scheme, the total reset time remains constant. In the proposed RWA scheme, the common bias voltage, V_b applied to the sustain (X) electrode can be adjusted to V_{b1} or V_{b2} during the first and second half of the address period on condition that a misfiring discharge can be prevented between the sustain (X) and scan (Y) electrodes. Since a lot of priming particles exist during the first half of the address period, the low scan voltage level, $V_{\text{scl}1}$ for the first half of the address period is increased to a low negative voltage level of -70 V when compared with the conventional low scan voltage $(\text{Vscl} = -100\ \text{V})$. The resultant common bias voltage, V_{b1} $(> V_{b2})$ is also slightly increased during the first half of the address period so as to compensate for the weak address discharge caused by the small potential difference between the scan (Y) and address (A) electrodes. The higher common bias voltage, V_{b1} $(> V_{b2})$ during the first half of the address period induces more wall charge accumulation at the initiation of the address discharge, as the voltage difference between the sustain (X) and scan (Y) electrodes is large. The low scan voltage level, $V_{\text{scl}2}$ in the second reset period should be lower than that in the first reset period so as to produce additional priming particles. As such, the low scan voltage level, $V_{\text{scl}2}$ in the second reset period is -100 V, which is exactly the same as that for the conventional waveform. As shown in the schematic diagram of electronic components of Fig. 6(b), the use of a low cost zener diode can generate the two different voltage levels, V_{scl1} and V_{scl2} for the proposed RWA driving scheme only with one additional FET element, in comparison with the electronic component for the conventional driving method with only one voltage level, V_{scl} in Fig. 6(a), which means that the additional driving cost rise for the RWA scheme is very small.

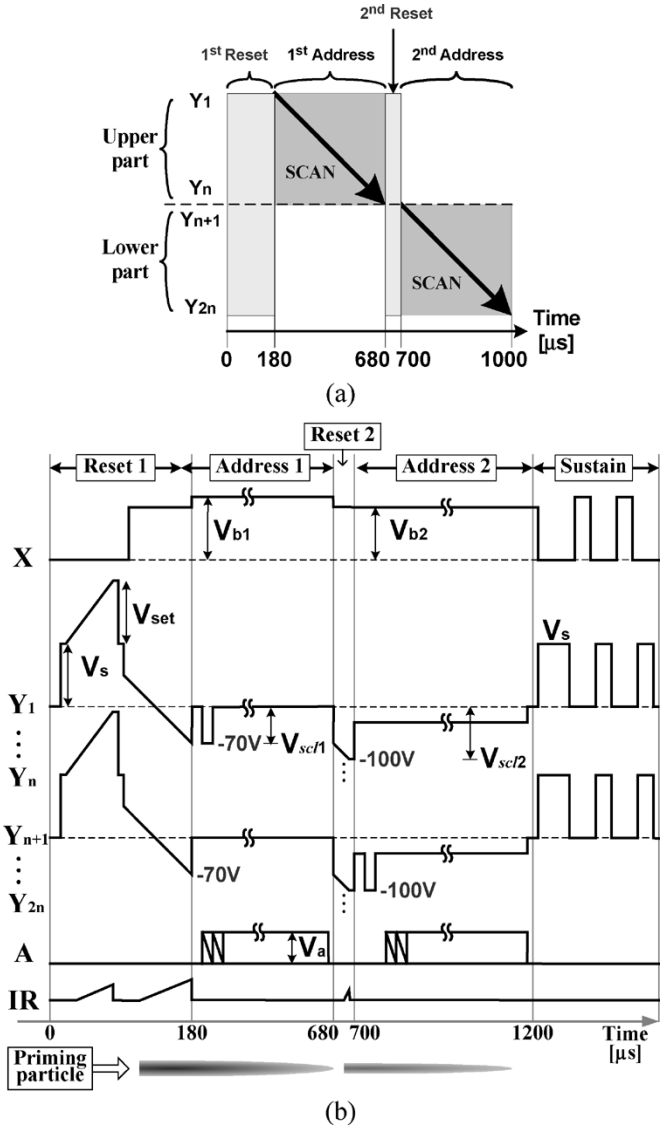

Fig. 5. (a) Schematic diagram of reset and address procedures and (b) corresponding driving waveforms with two groups and related IR emission and schematic diagram of priming particle distribution during address period with proposed RWA driving scheme.

Fig. 7(a)–(c) shows the IR (828 nm) emission waveforms measured during an address period at the (a) first, (b) middle, and (c) last scan time when applying the RWA driving waveforms with an address voltage of 70 V and scan pulsewidth of 1.0 μs. With the RWA driving scheme, the discharge time lags

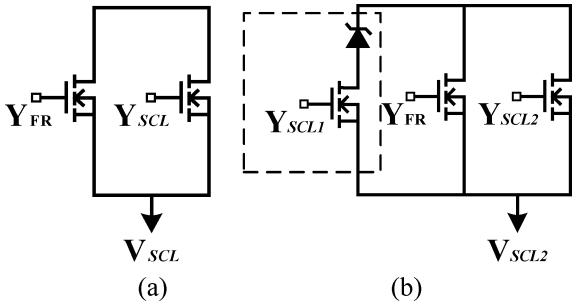

Fig. 6. Schematic diagram of electronic component for generating voltage level V_{scl} during address period. (a) Conventional scheme and (b) proposed RWA scheme.

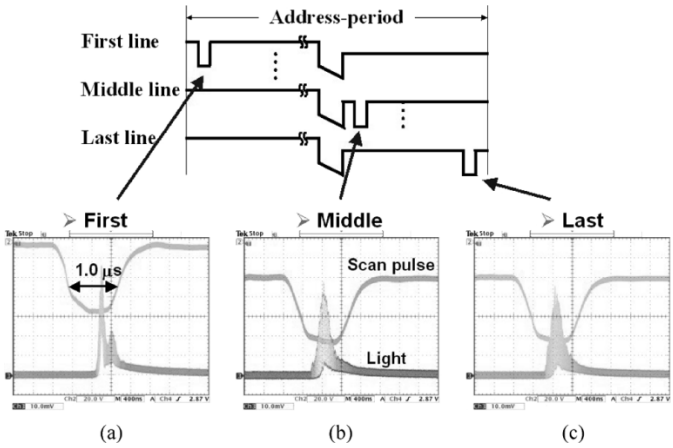

Fig. 7. Scan voltage and IR (828 nm) emission waveforms measured during address period at (a) first, (b) middle, and (c) last scan time, when applying RWA driving waveform with address voltage of 70 V and scan pulsewidth of 1.0 μs.

were shortened and the intensities of the IR emission were improved, especially for the middle and last scan time, when compared with the conventional address discharge shown in Fig. 3. Fig. 8 illustrates the changes in the address discharge time lags measured at the time intervals of 100 μs ranging from 200 to 1100 μs during an address period after the reset discharge when applying the proposed RWA driving waveforms with an address voltage of 70 V and scan pulsewidth of 1.0 μs shown in Fig. 5(b). The address discharge time lags of Fig. 8 during the first address period tended to increase slightly before 600 μs, which showed the almost same tendency as those of Fig. 4(b). During the second address period after the second reset discharge, the address discharge time lags also tended to increase slightly, which showed the almost same tendency as the address discharge time lags during the first address period in Fig. 8. This address discharge time lag phenomenon during the second address period is thought to be presumably due to the one more provision of the priming particles produced by the second reset discharge, as shown in the simple schematic density profile of the priming particles in the lower part of Fig. 5(b). Fig. 9 shows the comparison data of the address discharge time lags during the address period for both conventional [Fig. 2(b)] and RWA [Fig. 5(b)] driving cases. The address discharge time lags were significantly increased after 600 μs in the conventional case, yet for the proposed RWA driving scheme, the address discharge time lags were much decreased even after 600 μs, as shown in

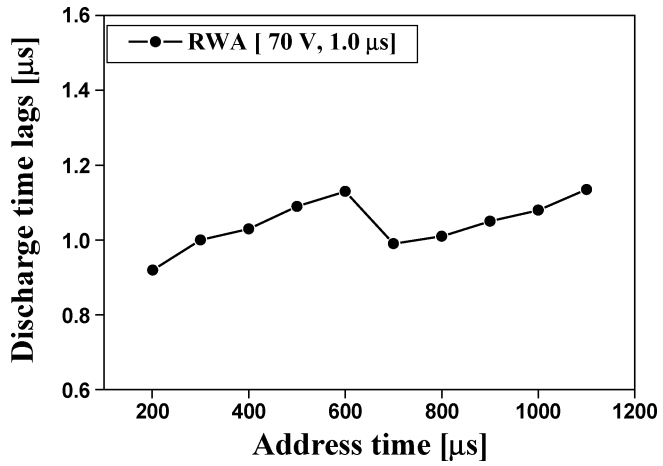

Fig. 8. Changes in address discharge time lags measured at time intervals of 100 μs ranging from 200 to 1100 μs during address period after reset discharge when applying proposed RWA driving waveforms with address voltage of 70 V and scan pulsewidth of 1.0 μs shown in Fig. 5(b).

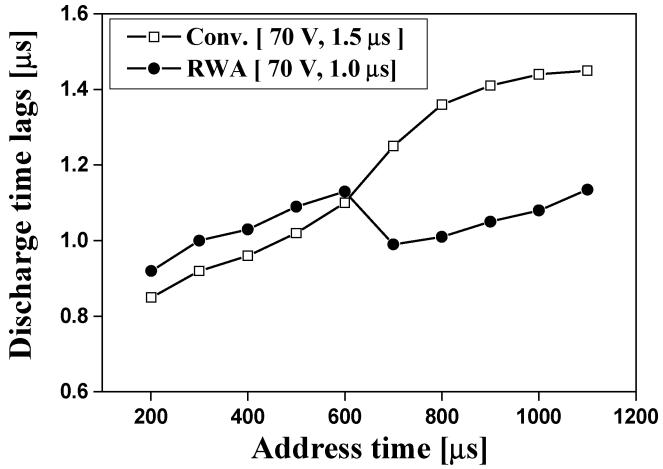

Fig. 9. Comparison data of address discharge time lags during address period for both conventional [Fig. 2(b)] and RWA [Fig. 5(b)] driving cases.

Fig. 9. The difference in the address discharge time lags between the conventional and RWA driving schemes was about 300 ns after 600 μs, confirming that the priming particles supplied by the falling reset ramp during the second reset period contributed to improving the address discharge characteristics in a high Xe gas environment after the first half of the address period.

Fig. 10(a) shows the scan waveforms before and after the second reset period in the upper and lower parts of the PDP. In the upper part of Fig. 10(a), the address discharges have already been produced prior to the application of the second reset waveform, whereas in the lower part of Fig. 10(a), no address discharges have been produced prior to the application of the second reset waveform. Note that the second reset waveform only affects the unaddressed cells in the lower part for an efficient second address discharge, that is, it does not affect the addressed cells in the upper part. Fig. 10(b) and (d) illustrates schematic wall charge models before and after the second reset period during an address period when using the proposed RWA driving scheme for the (b) upper and (d) lower parts, respectively. The wall charge model in Fig. 10(b) shows that the wall charge distribution already accumulated during the first address

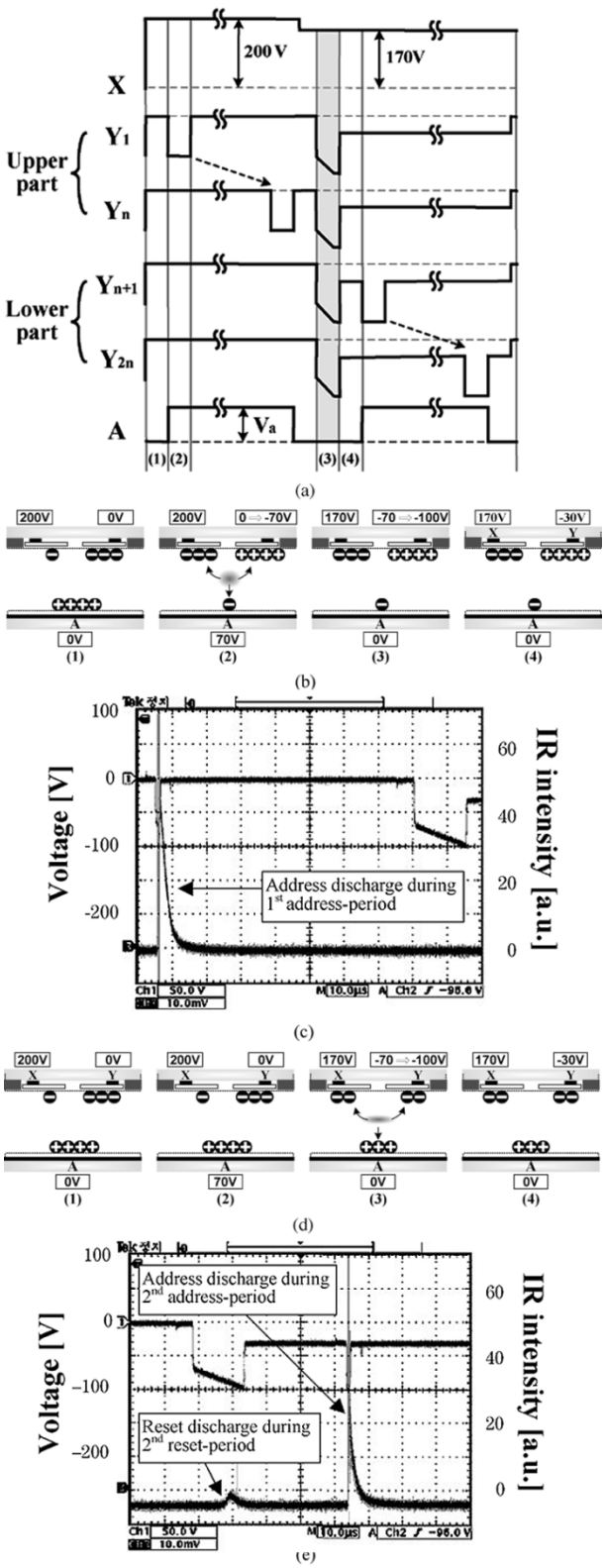

Fig. 10. (a) Scan waveforms before and after second reset period in upper and lower parts of PDP, corresponding schematic wall charge models before and after second reset period during first and second address periods of RWA driving scheme for (b) upper and (d) lower parts of PDP, and (c) and (e) experimental data for verifying wall charge models before and after second reset period during first and second address periods of RWA driving scheme.

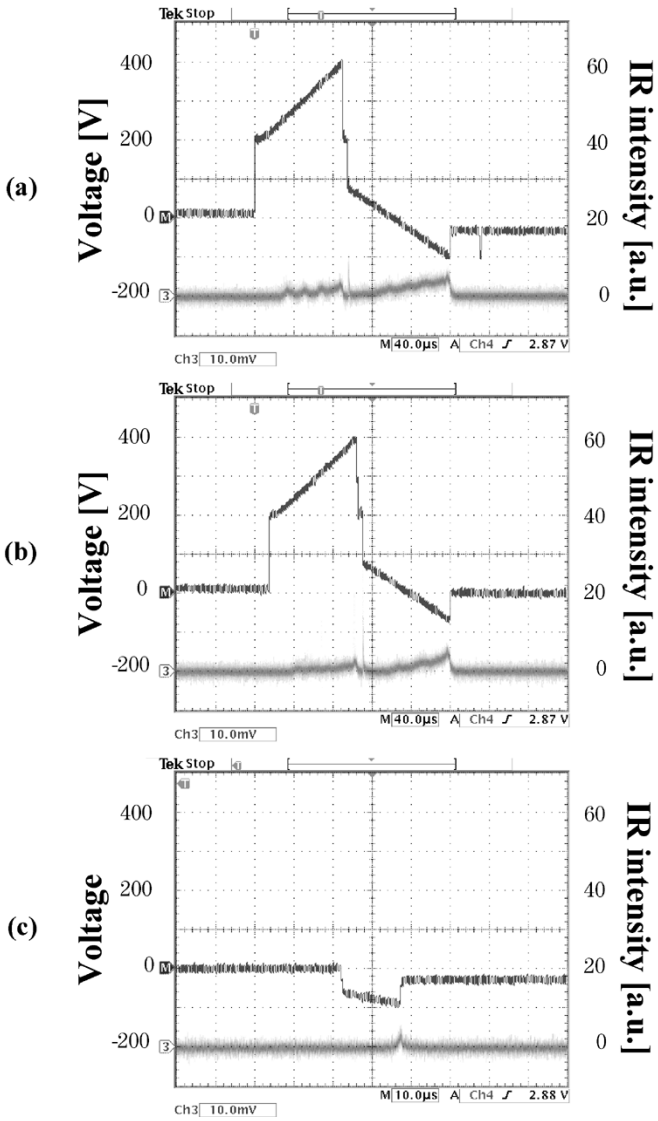

Fig. 11. IR (828 nm) emission waveforms during (a) conventional reset period in Fig. 2, (b) first reset period with proposed driving scheme in Fig. 5(b), and (c) second reset period with proposed driving scheme in Fig. 5(b).

period is not disturbed by the second reset discharge. When the first address discharge is produced before the second reset period, as shown in Fig. 10(b)-(2), that is, the address discharge occurs during the first address period, the ions are accumulated on the scan (Y) electrode. Accordingly, the positive wall charges on the scan (Y) electrode prevent any disturbance of the accumulated wall charges in the lower part by blocking any potential variation within the cells when the negative falling ramp pulse ranging from -70 to -100 V is applied in the second reset period, as shown in Fig. 10(b)-(3). Meanwhile, in the lower part, the second reset waveform plays the same role as the conventional reset waveform. The wall charge model of Fig. 10(b) is verified by the experimental measurement data of Fig. 10(c). As shown in Fig. 10(c), the IR emission is not detected when applying the second reset waveform in the cells where the address discharge occurs during the first address period shown in the IR emission of Fig. 10(c). As shown in Fig. 10(d), as there is no address discharge during the first address period, the polarity of the wall charges on the scan (Y) electrode in Fig. 10(d)-(2) is negative, thus a weak reset discharge is produced in the cells in the lower part with the application of the second reset waveform, as shown in Fig. 10(d)-(3). The resulting priming particles are

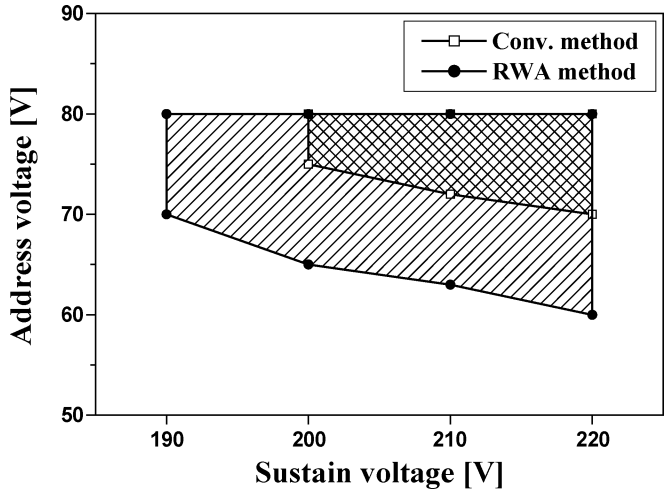

Fig. 12. Dynamic voltage margin measured for both conventional and proposed RWA driving schemes where width of address pulse is 1 μs.

TABLE II
COMPARISON OF MINIMUM ADDRESS VOLTAGE AND BACKGROUND LUMINANCE WHEN ADOPTING CONVENTIONAL AND RWA DRIVING SCHEMES

	Conventional	RWA
Minimum address voltage [V]	72	63
Background Luminance [cd/m^2]	0.12	0.12

produced prior to the second address discharge. The wall charge model of Fig. 10(d) is also verified by the experimental measurement data of Fig. 10(e). As shown in Fig. 10(e), the weak reset discharge is detected in the cells in the lower part with the application of the second reset waveform.

Fig. 11 shows the IR (828 nm) emission waveforms during (a) the conventional reset period in Fig. 2, (b) the first reset period with the proposed driving scheme in Fig. 5(b), and (c) the second reset period with the proposed driving scheme in Fig. 5(b). The results in Fig. 11 confirm that the background IR intensity of the proposed RWA driving scheme was almost the same as that of the conventional driving scheme. It was also observed that the resultant background luminance was the same for both the conventional and proposed driving schemes.

Fig. 12 shows the dynamic voltage margin measured for both the conventional and proposed RWA driving schemes where the width of the address pulse is 1 μs. As shown in the margin data of Fig. 12, the dynamic margin was enlarged considerably for the proposed RWA driving scheme, thanks to the providence of the priming particles through the second reset discharge during the second address period.

The minimum address voltage and background luminance were also measured when adopting the conventional and RWA driving waveforms and are listed in Table II. The results showed that the proposed RWA driving scheme reduced the minimum address voltage by about 9 V with a scan pulsewidth of 1.0 μs at the sustain voltage of about 210 V at a high Xe (15%) concentration under almost the same background luminance as the conventional case.

V. CONCLUSION

In this paper, we designed and examined a new RWA driving scheme to improve the address discharge characteristics with a high Xe gas mixture (15%) and thereby solve the conventional address problem of the gradual decrease in the priming particles during an address period. When compared with the conventional driving waveform, the RWA driving scheme successfully produced an address discharge within a 1.0 μs pulsewidth in an XGA grade PDP with a high Xe (15%) content due to the presence of priming particles throughout the address period. It is expected that the proposed RWA driving scheme can contribute to lowering the driving cost of the high efficient XGA grade PDP, thanks to the single scan addressing through the reduction of the address discharge time lags under the high Xe concentration.

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